

# MAEA-009445-000000

X-Band Phased Array Transmit / Receive Module (TRM)  
7-Bit Technology Demonstrator



2010 Data Sheet v1

The most important thing we build is trust

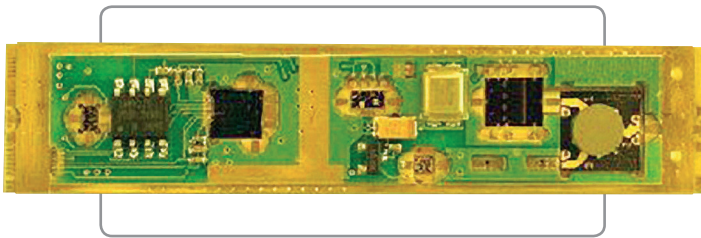
## Description

The X-Band 7-Bit TRM is an environmentally sealed module featuring full capability for phased array applications.

AESA requirements vary by application. The Cobham Sensor Systems TRM demonstrator shows our core design and manufacturing concepts which can then be tailored to the final application.

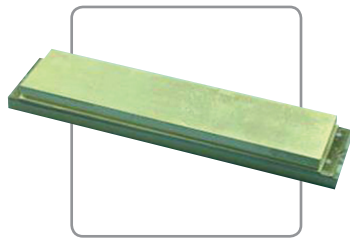
## Features

- Full Integration
- 10W HPA MMIC
- 1GHz Bandwidth
- Low noise figure (<4dB)
- 7 Bit serial Phase and Amplitude Control
- European Manufacture.



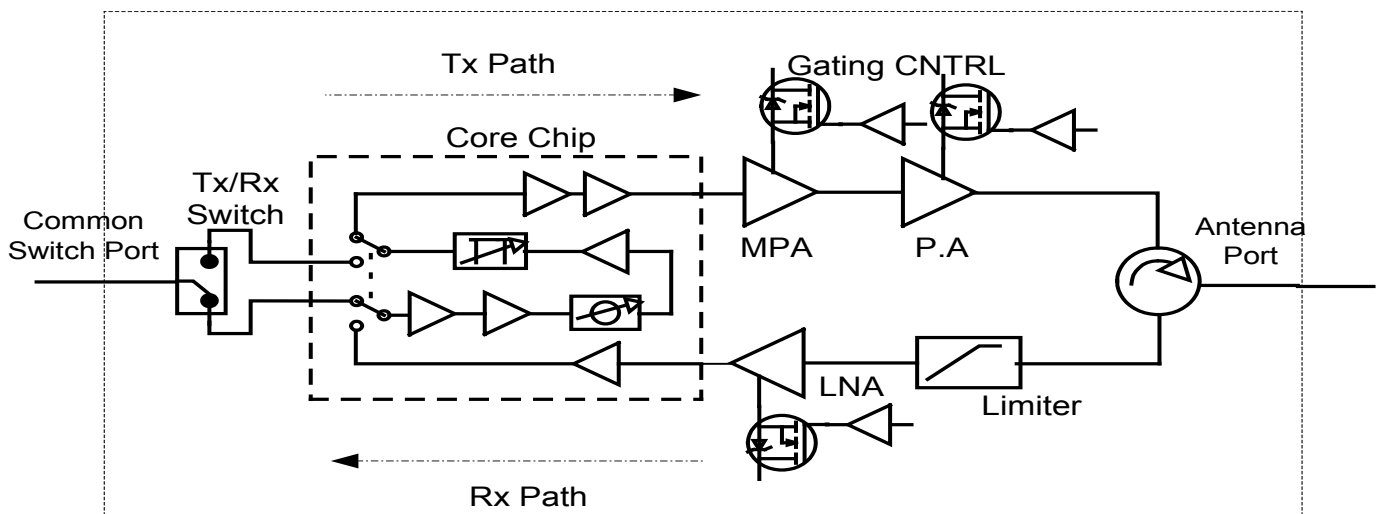
### Dimension

60.8 (L) x 13 (W) x 5.7 (H) mm



Parameter	Value	Units	
Frequency Band	9 ~ 10	GHz	
Output Power	8.5	W (peak)	
Operating Baseplate Temperature T <sub>OP</sub>	-40 ~ +50	°C	
Tx Input Power Level	+6	dBm	
Phase Control	0 - 360	Degrees (7 bits) 6° Resolution	
Attenuation Control Range	24	dB (7 bits) 0.4dB Resolution	
Noise Figure	< 4	dB	
Pulse Conditions	Pulse Width (max)	80	us
	Duty Cycle (max)	30	%

## TRM Functional Schematic



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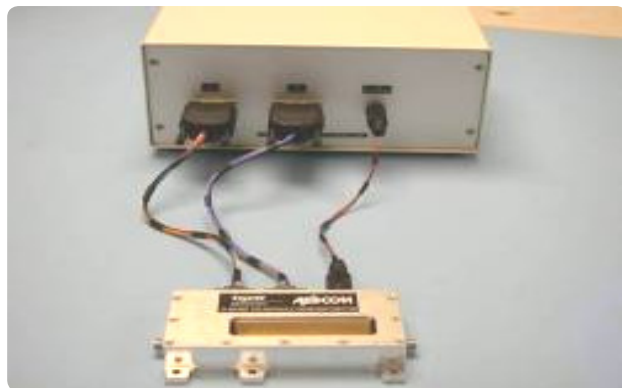
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## Description

The TRM demonstrator is supplied with:

- GUI control software
- Control & PSU Conditioning interface box
- PC to Control Box interface (LABJACK)
- TR Module in coax housing

train input to the control box, the modulator trigger, DC gating voltages for the driver amplifier, PA and Rx LNA are derived.



Further to this the end user must have access to the following equipment:

- +16v, -10v power supplies
- VNA (for Rx measurement)
- Peak Power Analyser (for Tx measurements)
- Pulse Generator
- Signal Generator
- RVA
- Modulator
- Host PC for GUI

The GUI provides a convenient way to control the functionality of the core chip. Tx / Rx mode and full phase/amplitude settings can easily be adjusted from the on-screen menu.

The control box performs the necessary supply conditioning required by the module. In addition to this, from a single pulse

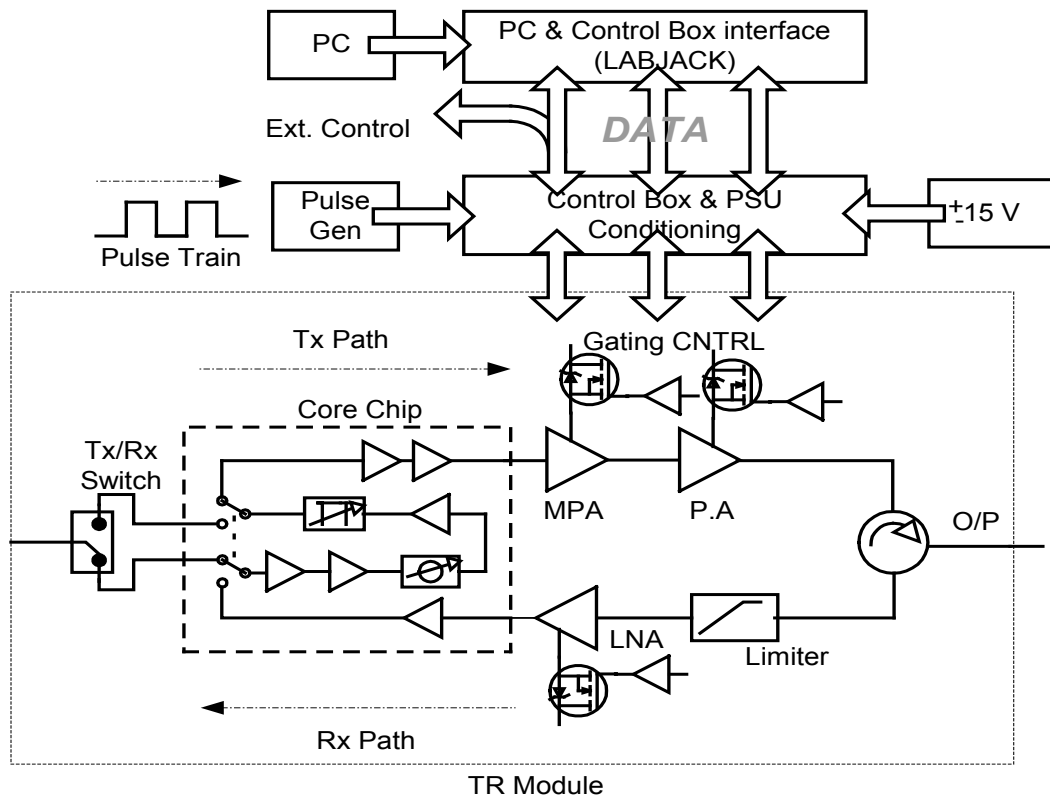
*Image shows TRM Demonstrator in housing with Control box*

Three modes of testing are possible with the TRM

- Continuous Receive Mode
- Continuous Transmit Mode
- Real - time transmit/receive Mode

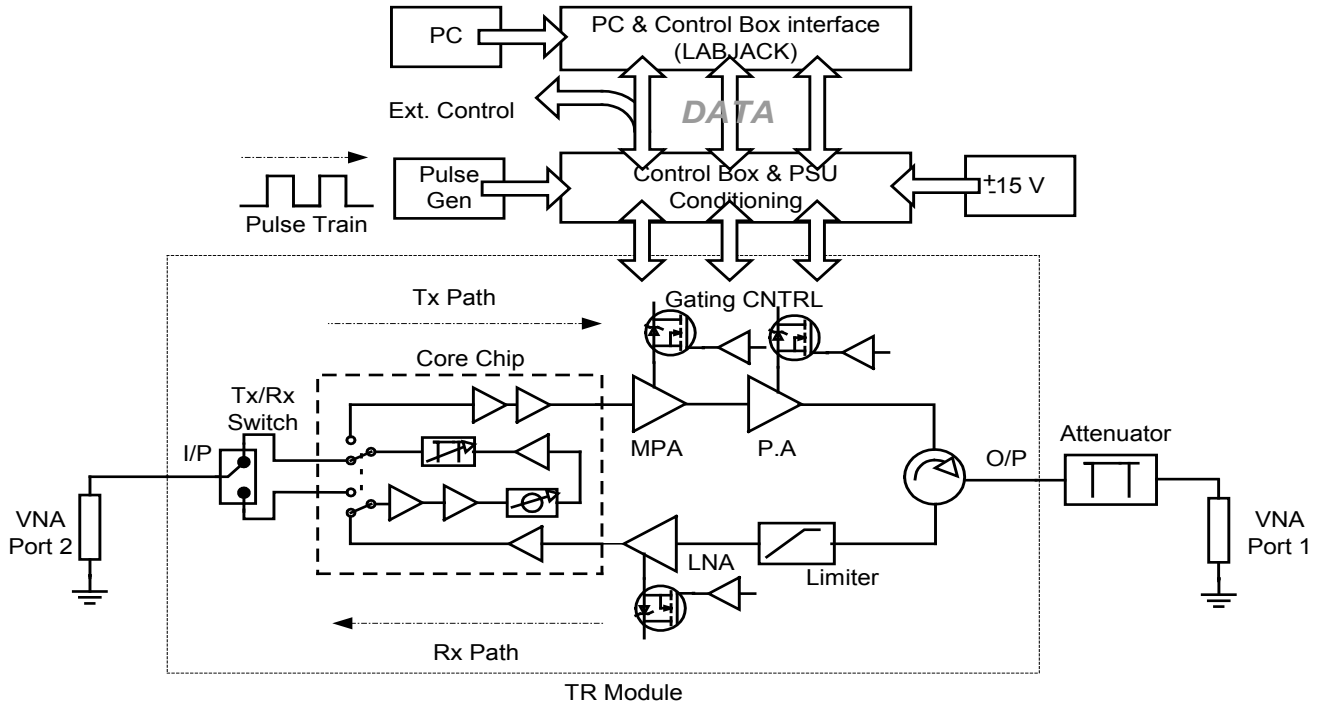
Continuous transmit and receive modes can easily be tested using this demonstrator kit, example test set-up's are shown on page 3 of this data sheet.

Real - time transmit/receive mode requires direct control of the core chip logic and MMIC gating. The control box provides external connections to enable the user full control w/o the host P.C. Enhanced user information can be found on page 4 onwards.

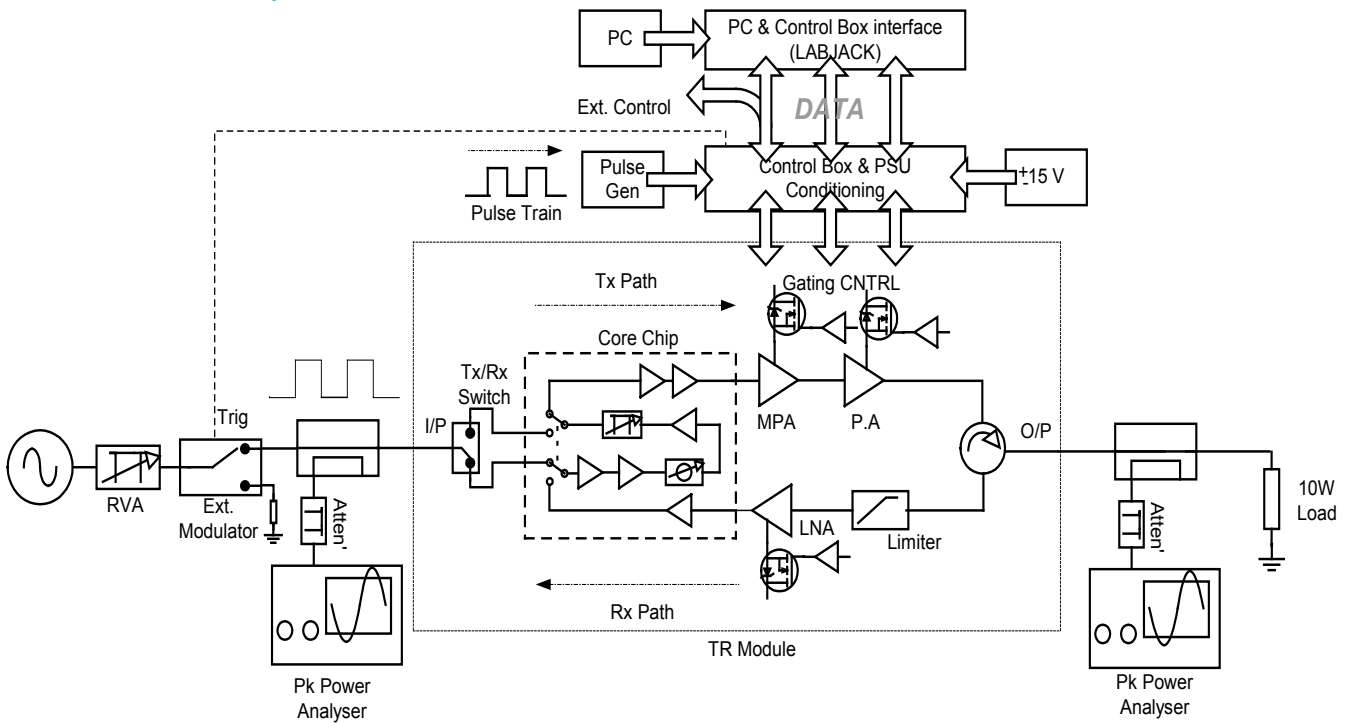


TRM Demonstrator Functional Control Set-up

## TRM Rx mode Test Set-Up



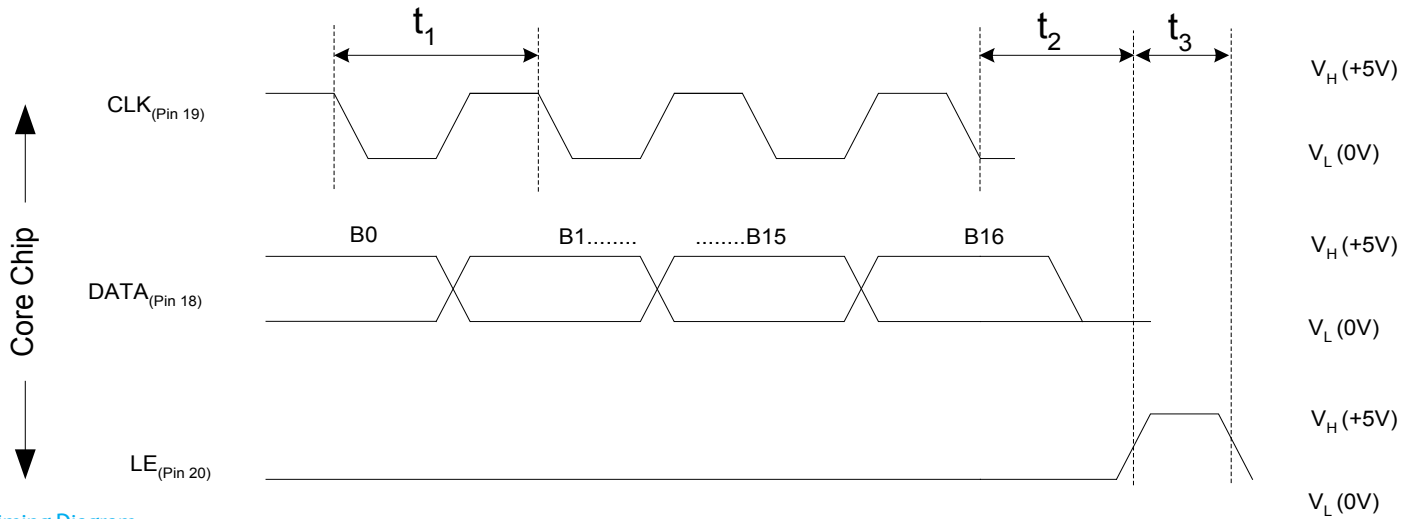
## TRM Tx mode Test Set-up



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## Core Chip Programming



### Timing Diagram

- Input Digital levels are CMOS and TTL compatible.
- Data is sampled at the falling edge of CLK.
- LE must occur when all bits are loaded and CLK is inactive.
- An extra CLK pulse is necessary at the end with no significant DATA (B16). Total of 17 CLK pulses.
- Upon re-programming all bits must be sent even if unchanged.

### Logic Truth Table

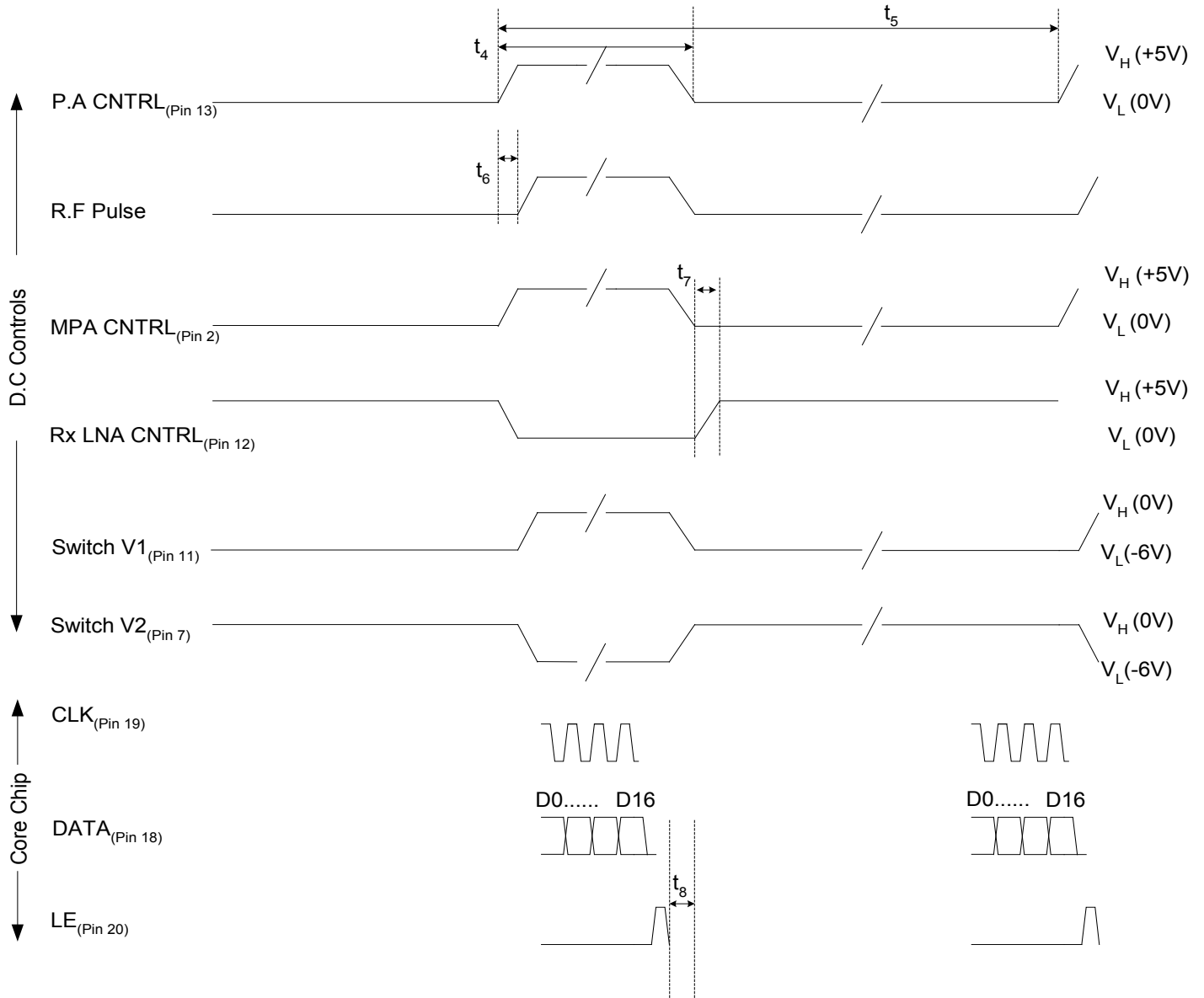
Bit Number	Description	Reference State	Nom. Value
B0	Phase shifter B6	High	178°
B1	Phase shifter B5	High	81°
B2	Phase shifter B4	High	52°
B3	Not Used		N/A
B4	Phase shifter B3	High	31°
B5	Phase shifter B2	High	16°
B6	Phase shifter B1	High	12°
B7	Phase shifter B0	High	6°
B8	Transmit/receive	High = transmit, Low = receive	N/A
B9	Attenuator B0	Low	0.4 dB
B10	Attenuator B1	Low	0.6 dB
B11	Attenuator B6	Low	11.3 dB
B12	Attenuator B5	Low	6.1 dB
B13	Attenuator B2	Low	1.1 dB
B14	Attenuator B4	Low	3.3 dB
B15	Attenuator B3	Low	1.9 dB
B16	End BIT	High	N/A

### Timing Characteristics

Parameter	Limit	Unit	Comment
$t_1$	4	nS min	Clock Rate
$t_2$	10	nS min	CLK to LE
$t_3$	8	nS min	LE Pulse Duration

- (1) Programming Rise & Fall times should be at least a factor of 10 times CLK period used.

## Timing Diagram



### Timing Characteristics

Param.	Limit	Unit	Comment
$t_4$	80	$\mu\text{S}$ max	P.A Drain voltage duration
$t_5$	266	$\mu\text{S}$ min	P.A Drain Inter pulse duration (30%Duty Tx)
$t_6$	1	$\mu\text{S}$ typ	P.A Drain D.C stability duration
$t_7$	TBD	nS max	Tx/Rx Switching Guard Time
$t_8$	200	nS max	Core Chip Response Time (From Falling Edge of LE Pulse)

(1) Control voltage Rise & Fall times: <5nS, 10% to 90%.

(2) Overshoot on control voltage lines should not exceed limits as specified on page 6.



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